

Memorandum

To: Senior Management
From: Rupesh Gajurel and Sriram Gopalakrisnan
Date: 4/13/2009
Re: Control Loop Design for Inverter

An analysis into the control aspect of the EDS inverter was done in order to design a controller that could meet the transient specification of the design.

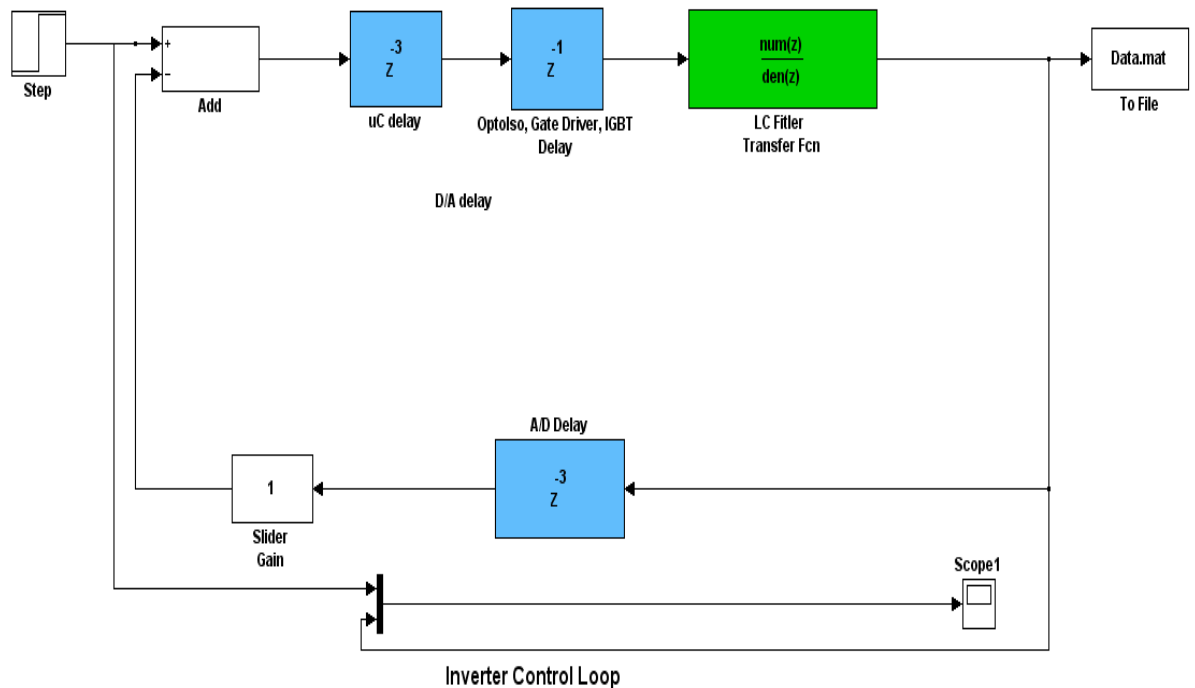


Figure 1: Inverter Closed Loop

According to initial estimation, the inverter loop consists of a microcontroller delay, the inverter hardware delay, the inverter filter, and a feedback A/D delay. The time step of the control loop is 100usec. It was estimated that the microcontroller (uC) delay would be maximum 300us, and the A/D delay would be around 300usec, which was taken from the data sheet. The Optoisolator, Gate Driver and IGBT delay was much less than 100usec but was estimated as 100usec just for a factor of safety. The step response of the closed loop is shown in

Figure 2. It is evident that the loop is unstable without any form of controller. The root locus of the inverter loop without controller is shown in Figure 3.

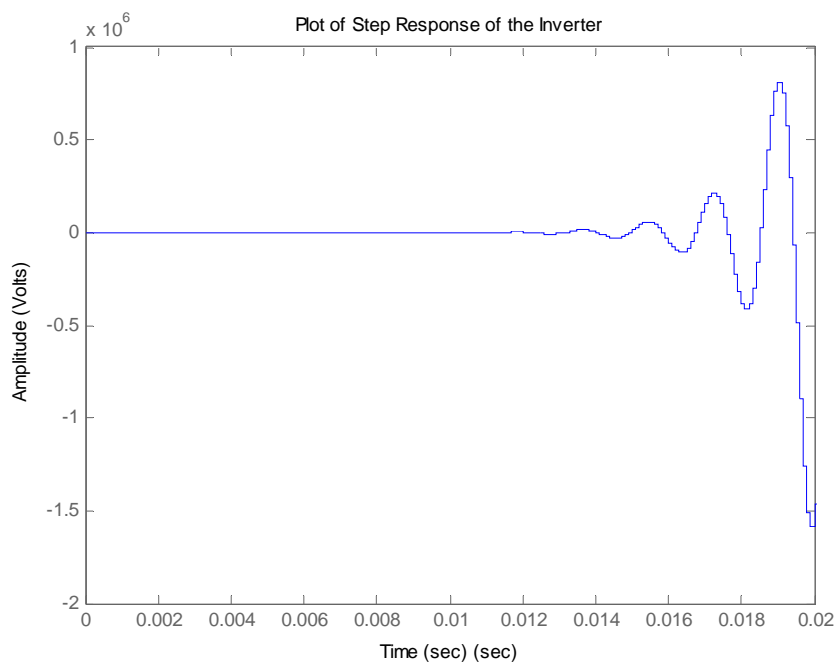


Figure 2

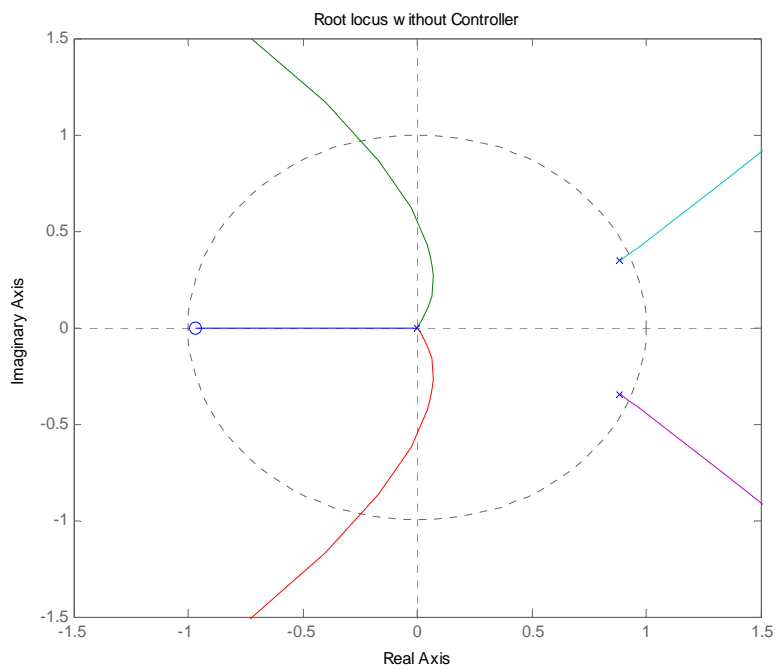


Figure 3

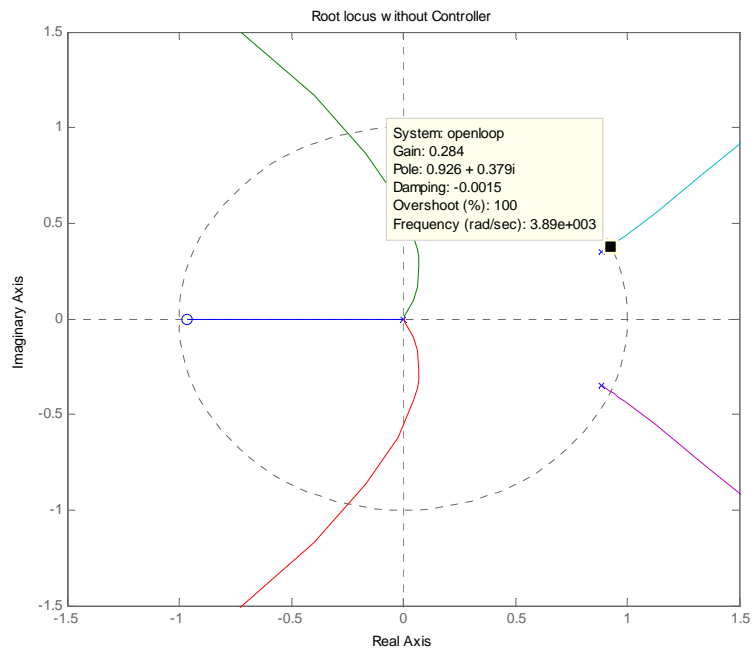


Figure 4

Figure 4 shows that for the system to be stable, the gain would have to be very small. The rightmost poles shown in Figure 4 are the poles due to the LC filter and these seem to be the dominant poles in the system. An integrator controller with a gain of 100 was added to stabilize the system. Figure 5 shows the root locus with an integrator.

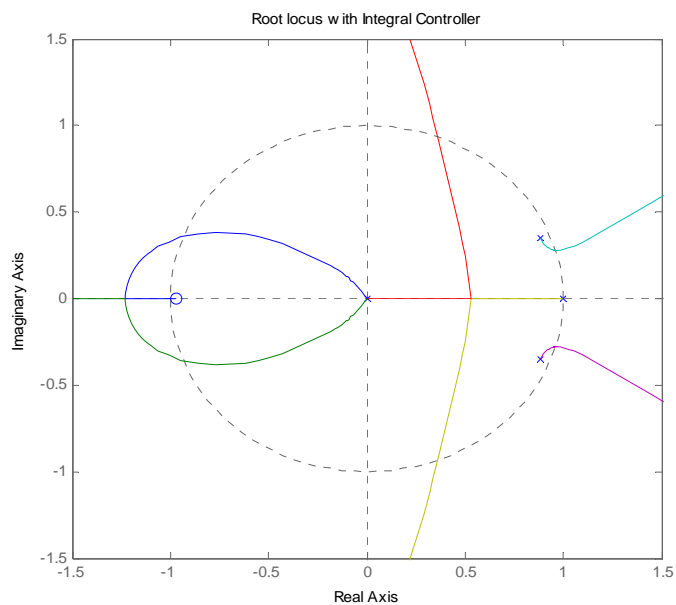


Figure 5

A gain of 100 on the integrator produced a step response shown in Figure 6. Figure 7 shows the Simulink block diagram for the full control loop.

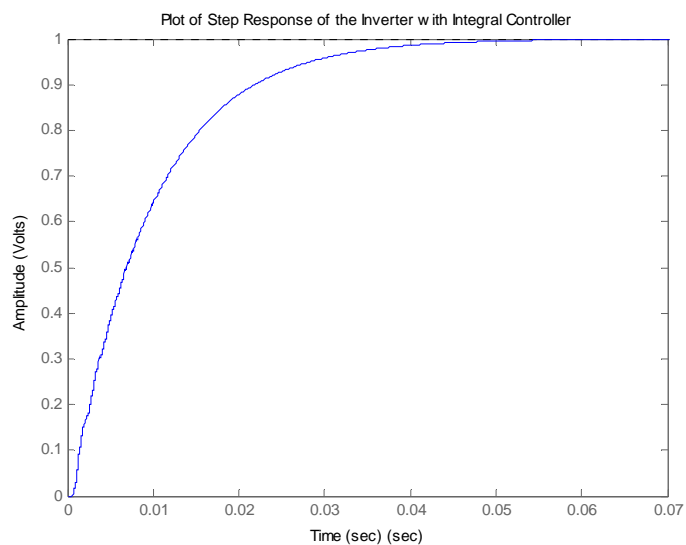


Figure 6

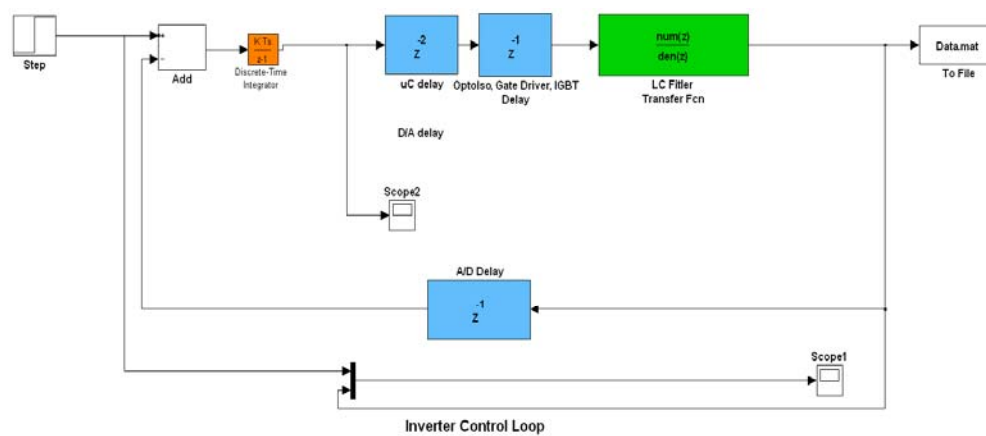


Figure 7

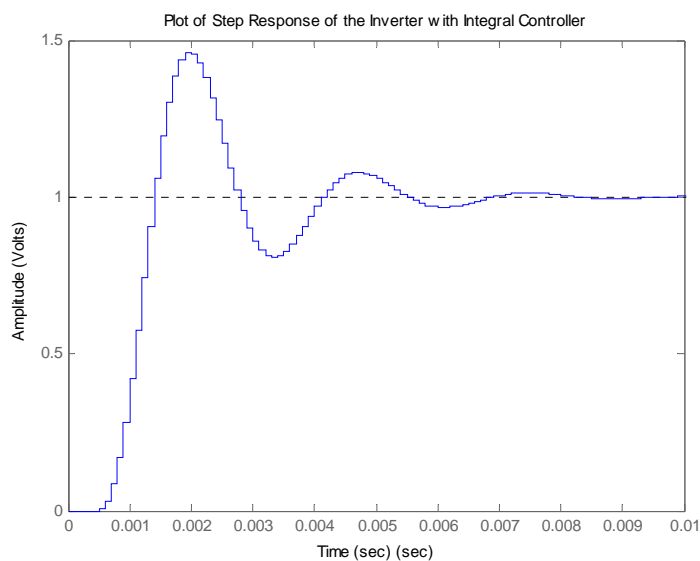


Figure 8: Step Response with $K = 1000$

Figure 8 shows the step response of the loop with 1000 as gain on the Integral Controller. Figure 9 shows the input reference sine and output sine for the same integral controller.

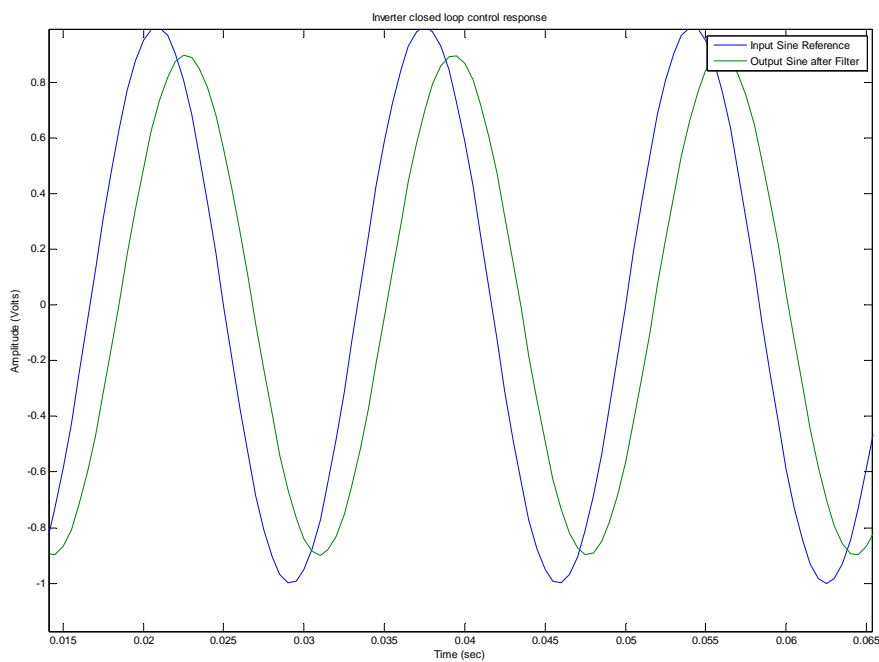


Figure 9

Conclusion: A simple Integrator controller with a gain of around 500 will be used to control the output of the Inverter. The total delay in the system was around 2ms.